

**SEMICONDUCTOR DEVICE WITH HEAT-DISSIPATING CAPABILITY
CROSS-REFERENCE TO RELATED APPLICATION**

This application is a continuation-in-part (CIP) of U.S. patent application serial no. 10/196,940, entitled
5 " A HIGH HEAT DISSIPATION MICRO-PACKAGING BODY FOR SEMICONDUCTOR CHIP", filed on July 18, 2002.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a semiconductor device, more
10 particularly to a semiconductor device with a heat-dissipating capability.

2. Description of the Related Art

Figure 1 illustrates a conventional semiconductor device 1 that includes a dielectric substrate 11, a
15 semiconductor chip 12 adhered on the dielectric substrate 11, a plurality of bonding wires 13 interconnecting electrically circuit traces on the dielectric substrate 11 and the semiconductor chip 12, a plurality of tin balls 16 mounted on a bottom surface
20 of the dielectric substrate 11, a heat-dissipating cover plate 14 covering the semiconductor chip 12 and the bonding wires 13, and a sealing resin 15 sealing a portion of the heat-dissipating cover plate 14 and a portion of the dielectric substrate 11. In the aforesaid
25 conventional semiconductor device 1, the heat-dissipating cover plate 14 does not contact the semiconductor chip 12 directly such that heat generated

by the semiconductor chip 12 cannot be effectively dissipated.

Figure 2 illustrates another conventional semiconductor device 2 disclosed in U.S. Patent No. 5,856,911. In the conventional semiconductor device 2, a dielectric substrate 21 is formed with a through hole. A heat-dissipating plate 22 is mounted on a bottom surface of the dielectric substrate 21. A semiconductor chip 23 is disposed in the through hole in the dielectric substrate 21, and is mounted on and is in thermal communication with the heat-dissipating plate 22. As such, heat generated by the semiconductor chip 23 can be dissipated by the heat-dissipating plate 22 and a heat sink 27 connected heat-conductively to the heat-dissipating plate 22. However, the number and arrangements of input/output terminals on the dielectric substrate 21 are limited by the size of the heat-dissipating plate 22. Furthermore, due to the presence of the heat sink 27, a circuit board 100 to be applied with the conventional semiconductor device 2 is required to be formed with a through hole for extension of the heat sink 27 therethrough.

Figure 3 illustrates a further conventional semiconductor device 3 disclosed in U.S. Patent No. 5,989,941. In the conventional semiconductor device 3, heat generated by a semiconductor chip 34 mounted on a dielectric substrate 31 is merely conducted to a

metallized circuit pattern 33 mounted on the dielectric substrate 31 via a plurality of bonding wires 35 such that the conventional semiconductor device 3 cannot achieve effective heat-dissipation.

5 Figure 4 illustrates still another conventional semiconductor device 4 disclosed in U.S. Patent No. 6,219,238B1. In the conventional semiconductor device 4, a heat-dissipating plate 42 is mounted on a top surface of a dielectric substrate 41. A semiconductor chip 43
10 is disposed in a through hole in the dielectric substrate 41 and is mounted on the heat-dissipating plate 42. A plurality of bonding wires 44 interconnect electrically the semiconductor chip 43 and a plurality of conductive contacts (not shown) on a bottom surface of the
15 dielectric substrate 41. As such, heat generated by the semiconductor chip 43 can be dissipated by the heat-dissipating plate 42. However, the number of input/output terminals, which can actually be formed on the bottom surface of the dielectric substrate 41,
20 is limited.

SUMMARY OF THE INVENTION

 Therefore, the object of the present invention is to provide a semiconductor device that can provide higher heat-dissipating efficiency as compared to the prior
25 art.

 According to the present invention, a semiconductor device comprises:

a dielectric substrate having opposite top and bottom surfaces and formed with a plurality of circuit traces, the top surface being formed with a plurality of first conductive contacts, each of which is connected
5 electrically to a corresponding one of the circuit traces, the bottom surface being formed with a plurality of second conductive contacts, each of which is connected electrically to a corresponding one of the circuit traces;

10 a heat-dissipating frame including an inner seat body mounted on the top surface of the dielectric substrate, an outer frame body mounted on the top surface of the dielectric substrate and surrounding and spaced apart from the inner seat body, and a plurality of
15 interconnecting portions, each of which interconnects heat-conductively the inner seat body and the outer frame body, the dielectric substrate cooperating with the inner seat body and the outer frame body so as to confine a surrounding groove, the first conductive contacts
20 being disposed in the surrounding groove;

a semiconductor chip mounted on and in thermal communication with the inner seat body, the semiconductor chip being provided with a plurality of contact pads thereon;

25 a plurality of bonding wires, each of which has one end connected electrically to one of the contact pads on the semiconductor chip, and the other end extending

into the surrounding groove and connected electrically to a corresponding one of the first conductive contacts on the top surface of the dielectric substrate so as to establish electrical connection between the contact pads on the semiconductor chip and the second conductive contacts on the bottom surface of the dielectric substrate via the first conductive contacts and the circuit traces; and

an encapsulant which encapsulates the bonding wires, the semiconductor chip, and the inner seat body, the interconnecting portions and a portion of the outer frame body of the heat-dissipating frame.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become apparent in the following detailed description of the preferred embodiment with reference to the accompanying drawings, of which:

Figure 1 is a schematic sectional view of a conventional semiconductor device;

Figure 2 is a schematic sectional view of another conventional semiconductor device;

Figure 3 is a schematic sectional view of a further conventional semiconductor device;

Figure 4 is a schematic sectional view of still another conventional semiconductor device;

Figure 5 is a schematic sectional view showing the preferred embodiment of a semiconductor device

according to the present invention;

Figure 6 is a schematic top view showing the preferred embodiment; and

5 Figure 7 is an exploded perspective view showing the preferred embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figures 5 to 7, the preferred embodiment of a semiconductor device 5, such as a ball grid array package, according to the present invention is shown
10 to include a dielectric substrate 51, a heat-dissipating frame 52, a semiconductor chip 53, a plurality of bonding wires 54, and an encapsulant 55.

The dielectric substrate 51 has opposite top and bottom surface 511, 512, and is formed with a plurality
15 of circuit traces 515. The top surface 511 is formed with a plurality of first conductive contacts 513, each of which is connected electrically to a corresponding one of the circuit traces 515 (see Figure 5). The bottom
20 surface 512 is formed with a plurality of second conductive contacts 514, each of which is connected electrically to a corresponding one of the circuit traces 515. The second conductive contacts 514 are adapted to be connected electrically to a circuit board (not
25 shown) via a plurality of tin balls 56 mounted respectively thereon.

The heat-dissipating frame 52 includes an inner seat body 522 mounted on the top surface 511 of the dielectric

substrate 51, an outer frame body 521 mounted on the top surface 511 of the dielectric substrate 51 and surrounding and spaced apart from the inner seat body 522, and a plurality of interconnecting portions 523, each of which interconnects heat-conductively the inner seat body 522 and the outer frame body 521. The dielectric substrate 51 cooperates with the inner seat body 522 and the outer frame body 521 so as to confine a surrounding groove 524, as best shown in Figure 5. The first conductive contacts 513 are disposed in the surrounding groove 524. In this embodiment, the heat-dissipating frame 52 is made of a material selected from the group consisting of copper and copper alloy. The inner seat body 522 has a thickness less than that of the outer frame body 521, and is rectangular. The interconnecting portions 523 extend upwardly and inclinedly from corners of the inner seat body 522, as shown in Figures 5 and 6. Each interconnecting portion 523 is formed with a silver plating or a gold plating for enhancing heat conductivity.

The semiconductor chip 53 is mounted on and is in thermal communication with the inner seat body 522. The semiconductor chip 53 is provided with a plurality of contact pads 531 thereon.

Each bonding wire 54 has one end 541 connected electrically to one of the contact pads 531 on the semiconductor chip 53, and the other end 542 extending

into the surrounding groove 524 and connected electrically to a corresponding one of the first conductive contacts 513 on the top surface 511 of the dielectric substrate 51 so as to establish electrical connection between the contact pads 531 on the semiconductor chip 53 and the second conductive contacts 514 on the bottom surface 512 of the dielectric substrate 51 via the first conductive contacts 513 and the circuit traces 515.

The encapsulant 55 encapsulates the bonding wires 54, the semiconductor chip 53, and the inner seat body 522, the interconnecting portions 523 and a portion of the outer frame body 521 of the heat-dissipating frame 52.

In view of the configuration of the heat-dissipating frame 52, heat generated by the semiconductor chip 53 can be rapidly and effectively conducted to the outer frame body 521 via the inner seat body 522 and the interconnecting portions 523, and is then dissipated. Furthermore, since the outer frame body 521 is mounted on the top surface 511 of the dielectric substrate 51 and since the surrounding groove 524 permits extension of the bonding wires 54 therethrough, the number and locations of the second conductive contacts 514 on the bottom surface 512 of the dielectric substrate 51 are not restricted.

While the present invention has been described in

connection with what is considered the most practical and preferred embodiment, it is understood that this invention is not limited to the disclosed embodiment but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation so as to encompass all such modifications and equivalent arrangements.